WHAT IS CLAIMED IS:

1. A Delay Locked Loop DLL circuit comprising:

a first delay circuit for delaying an input clock signal to output a plurality of delayed clock signals;

a first selector for selecting a first delayed clock signal and a second delayed clock signal from among the plurality of delayed clock signals, for output;

a second delay circuit for delaying the input clock signal to generate a slightly delayed clock signal;

a second selector for selecting two selected clock signals from among the slightly delayed clock signal, the first delayed clock signal, and the second delayed clock signal, for output; and

a delay synthesis circuit for generating an internal clock signal from said selected clock signals, for output.

2. The DLL circuit according to claim 1, wherein a delay time during which the slightly delayed clock signal is generated from the input clock signal is shorter than a sum of a delay time of said first delay element and a delay time of said first selector.

3. The DLL circuit according to claim 1, wherein the slightly delayed clock signal includes M slightly delayed signals, where M is an integer of at least one, and M + 2 is smaller than a number N of said plurality of delayed clock signals.

4. The DLL circuit according to claim 1, wherein said first delay circuit includes first to Nth delay elements;

said input clock signal is supplied to an input terminal of said

first delay element;

an output terminal of the ith delay element, where i is an arbitrary natural number not more than N - 1, is connected to an input terminal of an (i + 1)th delay element; and

said first selector selects the clock signals output from output terminals of the mth delay element and an (m + 1)th delay element, respectively, as a first delayed clock signal and a second delayed clock signal, for output, where m is a number selected from among natural numbers of at least one and not more than N - 1.

5. The DLL circuit according to claim 4, wherein a delay time during which the slightly delayed clock signal is generated from the input clock signal is smaller than a sum of a delay time of said first delay element and a delay time of said first selector.

6. The DLL circuit according to claim 2, wherein

the slightly delayed clock signal includes M slightly delayed clock signals, where M is an integer of at least one;

said second delay circuit includes first to Mth delay devices for respectively generating the slightly delayed clock signals from the input clock signal;

delay times of the second to said Nth delay elements are identical; and

a delay time td_j of the jth delay device among said first to said Mth delay devices, where j is an arbitrary natural number not more than M, is expressed, using a delay time Td2 of said first delay element, a Td3 of said first selector, and delay times Td5 of said second to said Nth

delay elements:

$td_j = Td2 + Td3 - j \cdot Td5$.

7. A DLL circuit comprising:

an input buffer for receiving an external clock signal and then generating an input clock signal;

a first delay circuit for delaying the input clock signal to output a plurality of delayed clock signals;

a first selector for selecting a first delayed clock signal and a second delayed clock signal from among the plurality of delayed clock signals, for output;

a second delay circuit for delaying said input clock signal to generate a first slightly delayed clock signal;

a third delay circuit for delaying an external clock signal to generate a second slightly delayed clock signal;

a second selector for selecting two selected clock signals from among the first slightly delayed clock signal, the second slightly delayed clock signal, the first delayed clock signal, and the second delayed clock signal, for output; and

a delay synthesis circuit for synthesizing an internal clock signal from the selected clock signals, for output.

8. The DLL circuit according to claim 7, wherein a delay time during which the first slightly delayed clock signal is generated from the input clock signal is shorter than a sum of a delay time of said first delay element and a delay time of said first selector; and

a delay time during which the second slightly delayed clock

signal is generated from the external clock signal is smaller than a sum of a delay time of said input buffer and a delay time during which the first slightly delayed clock signal is generated from the input clock signal.

9. The DLL circuit according to claim 7, wherein said first delay circuit includes first to Nth delay elements;

the input clock signal is supplied to an input terminal of said first delay element;

an output terminal of the ith delay element, where i is an arbitrary natural number no more than N – 1, is connected to an input terminal of the (i + 1)th delay element; and

said first selector selects the clock signals output from an output terminal of the mth delay element, where m is a number selected from among natural numbers of at least one and not more than N – 1, and an output terminal of an (m + 1)th delay element among said first to said Nth delay elements as the first delayed clock signal and the second delayed clock signal, for output.

10. The DLL circuit according to claim 9, wherein delay times of the second to said Nth delay elements are identical;

the first slightly delayed clock signal includes M first slightly delayed clock signals, where M is an integer of at least one;

the second slightly delayed clock signal includes M' second slightly delayed clock signals, where M' is an integer of at least one;

said second delay circuit includes first to Mth delay devices for respectively generating the first slightly delayed clock signals;

said third delay circuit includes first to M'th slightly delay devices for respectively generating the second slightly delayed clock signals; and

a delay time td_j of the jth delay device among said first to said Mth delay devices, where j is a natural number of not more than M, and a delay time td_k of the kth slight delay device among said first to said M'th slight delay devices, where k is a natural number of not more than M' are expressed by following formulas, using a delay time Td1 of said input buffer, a delay time Td2 of said first delay element, a delay time Td3 of said first selector, and delay times Td5 of said second to said Nth delay elements:

$$td_j = Td2 + Td3 - j \cdot Td5,$$

$$td_k' = Td1 + Td2 + Td3 - (M + k) \cdot Td5.$$

11. The DLL circuit according to claim 1, wherein said delay synthesis circuit generates the internal clock signal from the selected clock signals, for output, so that a rise timing of the internal clock signal is between rise timings of the selected clock signals, and a fall timing of the internal clock signal is between fall timings of the selected clock signals.

12. The DLL circuit according to claim 7, wherein said delay synthesis circuit generates the internal clock signal from the selected clock signals, for output, so that a rise timing of the internal clock signal is between rise timings of the selected clock signals, and a fall timing of the internal clock signal is between fall timings of the selected clock signals.